



Procedures and Guidelines

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Title: Electronics Design and Development Guidelines

1. PURPOSE

This procedure establishes guidelines for providing electronics design and development in support of in-house GSFC products.

2. REFERENCE

GPG 1310.1, Customer Commitments and Review
GPG 1710.1, Corrective and Preventive Action
GPG 5330.1, Product Processing, Inspection, and Test
GPG 5340.2, Control of Non-conforming Product
GPG 8700.1, Design Planning and Interface Management
GPG 8700.2, Design Development
GPG 8700.3, Design Validation
GPG 8700.4, Technical Review Program
GPG 8730.3, The GSFC Quality Manual
500-PG-1310.1.1, External Customer Agreements
500-PG-8700.2.3, Issue and Management of Engineering Drawing Numbers
500-PG-8700.2.5, Engineering Drawing Standards Manual

3. SCOPE

This procedure establishes guidelines for Product Design Team (PDT) members providing electronics design and development support to GSFC products covered by the scope of the GSFC Quality System.

4. DEFINITIONS

- a. Product Design Lead (PDL) – The PDL is the manager or leader responsible for managing the design activity, managing the technical and organizational interfaces identified during design planning, and where required, forming and leading the Product Design Team (PDT). The term PDL may refer to flight project managers, mission managers, instrument managers, subsystem technical managers, integrated product development team leaders, lead engineers, or others who have the responsibility for managing a design activity. In the context of this document, PDL refers to a lead engineer.
- b. Customer - Any organization or person receiving electronics design and development support from the AETD.

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5. AUTHORITIES AND RESPONSIBILITIES

The PDL, hereafter referred to as the lead engineer, is responsible for the quality and timely completion of the electronics design and development activities as specified in the Customer Agreement and/or Statement of Work (SOW) (see GPG 1310.1, Customer Commitments and Review; and 500-PG-1310.1.1, External Customer Agreements). This includes providing the design output (documentation including engineering drawings, test plans, procedures, and reports), budgets, schedules, and review support to the customer. It is the responsibility of the lead engineer, in partnership with the customer, to determine and document in an implementation plan (per GPG 8700.1, Design Planning and Interface Management) which specific steps of the typical electronics design and development process (as described herein) will be executed.

6. CANCELLATION

500-PG-8700.2.2, Electronics Design and Development Guidelines

7. RECORDS

Quality Record Title	Record Custodian	Retention
Implementation Plan	Lead Engineer, then Project Office (at completion of development activity)	NASA Records Retention Schedule (NRRS) 1/22A. Permanent. Retire to a Federal Records Center (FRC) when 5 years old. Transfer to NARA when 10 years old.
Work Order Authorization (WOA)	Lead Engineer, then Project Office (at completion of development activity)	NRRS 8/5A2. Project Test, Engineering, and Evaluation Files. Records may be retired to an FRC when 2 years old. Destroy when 15 years old.
Design Verification Test Reports and/or Summaries	Lead Engineer, then Project Office (at completion of development activity)	NRRS 8/5A2.
Review Summaries, Requests for Action (RFA's), and Responses	Project Office	NRRS 7/5B1. Permanent. Document may be retired to an FRC 1 year after publication. Transfer to NARA when 25 years old.
Configuration Management Records	Performing Organization	NRRS 8/5A2.

8. IMPLEMENTATION

The following procedure describes the typical process for providing electronics design and development support to a customer. The actual process is by nature iterative and must maintain some degree of flexibility.

8.1 Compilation of Design Inputs

The lead engineer/PDT shall compile and evaluate the design inputs which may include one or more of the following:

- Statement of Work
- Customer-imposed requirements
- Interface Control Drawings
- Applicable specifications, standards, and statutory/regulatory requirements
- Any other AETD imposed requirements

8.2 Initial Planning

8.2.1 The lead engineer shall develop an implementation plan which contains a high level description of the electronics hardware to be developed, key support personnel, a budget, and a schedule for review and approval by the customer. The plan should include adequate contingencies for completion of the design and development activity within the resources negotiated in the Customer Agreement and/or SOW. The implementation plan shall be maintained per the applicable configuration management plan.

8.2.2 The lead engineer and his/her organizational supervisor shall ensure that the PDT is composed of individuals, civil servants and/or contractors as necessary, with the required discipline skills.

8.3 Requirements Definition

The lead engineer generates a requirements document from the design inputs. It may be necessary for the PDT to perform various analyses in order to derive lower level design requirements from the top level design inputs. These top level and derived requirements shall be documented, reviewed for adequacy, and approved by the customer. The requirements document shall be maintained per the applicable configuration management plan.

8.4 Design Practice

The design effort shall be conducted according to the following good design practices, as appropriate:

8.4.1 Multiple design concepts should be identified, and the best selected by a trade study process. The best design concept is that which meets all of the design requirements and has the best combination of low cost, least technical complexity, and minimal schedule risk. (Other factors, such as design heritage, may also influence the final choice.) For instance, it may be necessary to prototype one or more of the design options and to conduct various performance and/or

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environmental tests before the optimum design path is chosen. In any case, the customer shall be a key participant in this critical selection process. In addition, the results of the trade study process are typically "peer reviewed" (see GPG 8700.4, Technical Review Program).

- 8.4.2 Detailed designs should be as simple as possible, making maximum use of standardization, repeated elements, known processes, and readily available parts and materials.
- 8.4.3 Designs, as well as the specific parts incorporated into designs, should be robust and insensitive to typical and/or expected environmental conditions (e.g. radiation environment, thermal variations, etc.).
- 8.4.4 All appropriate functional discipline personnel (e.g. manufacturing, integration, testing, and other subsystems) having interfaces or involvement to be considered should be a part of the PDT, or, as a minimum, be consulted to make suggestions to improve manufacturability, testability, etc. and/or reduce the costs associated with such activities. The lead engineer shall decide whether to accept or reject these recommendations.
- 8.4.5 Final product designs shall be documented using standard GSFC electronics drawing practices per 500-PG-8700.2.5, the Engineering Drawing Standards Manual. Typical product documentation sets include electronic schematics, wiring diagrams, parts lists, and assembly drawings. Instructions for obtaining official GSFC drawing numbers can be found in 500-PG-8700.2.3, Issue and Management of Engineering Drawing Numbers. The drawing practices in 500-PG-8700.2.5 may also be applicable to pre-flight and pre-operational hardware (such as engineering test units, breadboards, and proof-of-concept hardware), but are not required. Applicability shall be determined by the lead engineer.
- 8.4.6 The following checklist of electronics design considerations is provided as an aid in generating and implementing the design:
- application (spaceflight, ground, aircraft, balloon, sounding rocket, etc.)
 - timing margins
 - environmental conditions (thermal, radiation, vibration, etc.)
 - power/thermal dissipation
 - electro-magnetic interference (EMI), electro-magnetic compatibility (EMC)
 - parts classification
 - parts application in design (e.g. radiation, life considerations)
 - packaging strategy
 - testability
 - ground support equipment

8.5 Design Changes

Design changes, as required by customer request, process improvement, errors in the original design, improper component selection, drawing error, product non-conformance, etc., shall be documented, approved, and implemented per the relevant configuration management plan. Lead engineers shall be familiar with the customer's configuration management process, such as how changes are requested,

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reviewed, and approved, as well as forms, web sites, or other media utilized in the process.

8.6 Design Reviews

At appropriate stages throughout the electronics design and development process, reviews shall be scheduled and conducted.

- 8.6.1 Internal reviews are held during the design process and are truly at the grass roots level. Participants of these informal reviews are usually PDT members and other electronics engineers. Though not required, informal documentation and tracking of action items sometimes occurs at the discretion of the lead engineer.
- 8.6.2 Peer Reviews (per GPG 8700.4, Technical Review Program) are more formal reviews that evaluate a design's technical status using a team of appropriate specialists independent of the PDT. Emphasis is placed on selecting a well-rounded review team consisting of personnel cognizant of and experienced with the subject matter of the review. These reviews are conducted to ensure that the electronics design meets the design requirements. It is the responsibility of the lead engineer and/or PDT to respond to all action items, recommendations, and comments generated at these reviews. The reason for holding a Peer Review could be any one or more of the following:
- Required by the customer's peer review plan
 - Review of a new design
 - Review results of trade study
 - Review modifications to an existing design or to existing design requirements
 - Preparation for a System Review
 - Preparation for a functional test, environmental test, or shipment of hardware
- 8.6.3 System Reviews (See GPG 8700.4, Technical Review Program) are formal, technical reviews that systematically evaluate a project's technical status. They are conducted as specified in the project's systems review plan, but typically include such reviews as the System Concept Review, Preliminary Design Review, Critical Design Review, Pre-Environmental Test Review, and Pre-Ship Review. The lead engineer/PDT often participate in the System Review process by preparing and/or presenting presentation material, and/or preparing responses to action items.

8.7 Design Verification

During the engineering design and development process, design verification shall be conducted as required to ensure that the design meets the customer's requirements. Verification consists of analysis, review, and/or testing.

- 8.7.1 Depending upon the application, performing one or more of the following analyses may be appropriate:
- Various circuit analyses (simulation, timing, EMC, parts stress, etc.)
 - Circuit, board, or box level thermal and/or structural analysis
 - Comparison with similar systems/designs

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- 8.7.2 In addition to internal reviews, Peer and Systems Reviews will be conducted as described in Section 8.6 of this procedure to verify that the design and test documentation meets the customer's requirements.
- 8.7.3 Development and testing of proof-of-concept designs, breadboards, engineering test units, and life test units may also be conducted as part of design verification.
- 8.7.4 The Work Order Authorization (WOA) shall be utilized (per GPG 5330.1, Product Processing, Inspection, and Test) to plan and document inspection and test events, including all functional and environmental tests, required for design verification.

8.8 Design Validation

The lead engineer/PDT shall validate the product in accordance with GPG 8700.3, Design Validation. Note that validation includes manufacture, integration to larger systems/assemblies, as well as environmental and functional tests. Also note that due to the iterative nature of the design process, intermediate validation is frequently required.

- 8.8.1 The lead engineer shall determine the most appropriate and efficient method for fabrication of the hardware. Options include use of in-house manpower, task order contracts, or any other contracting medium that accesses a viable fabrication resource.
- 8.8.2 Assembly of spaceflight electronics shall be performed in accordance with an assembly drawing and/or plan, and shall be performed under the appropriate environmental conditions. Some items for consideration are:
- Cleanliness requirements
 - Temperature/humidity requirements
 - Electro-static discharge (ESD) control
 - Adequacy of space
- 8.8.3 Validation testing shall be conducted using approved (formally released) validation test plans and procedures. Validation shall consist of the following, as appropriate:
- Interface testing (mechanical and electrical)
 - Functional testing
 - Life testing
 - Vibration testing
 - Thermal/Vacuum testing
 - Thermal Balance testing
 - EMI/EMC testing
 - Magnetic testing
- 8.8.4 The WOA shall be utilized (per GPG 5330.1, Product Processing, Inspection, and Test) to plan and document manufacturing, assembly, inspection, and test events, including all functional and

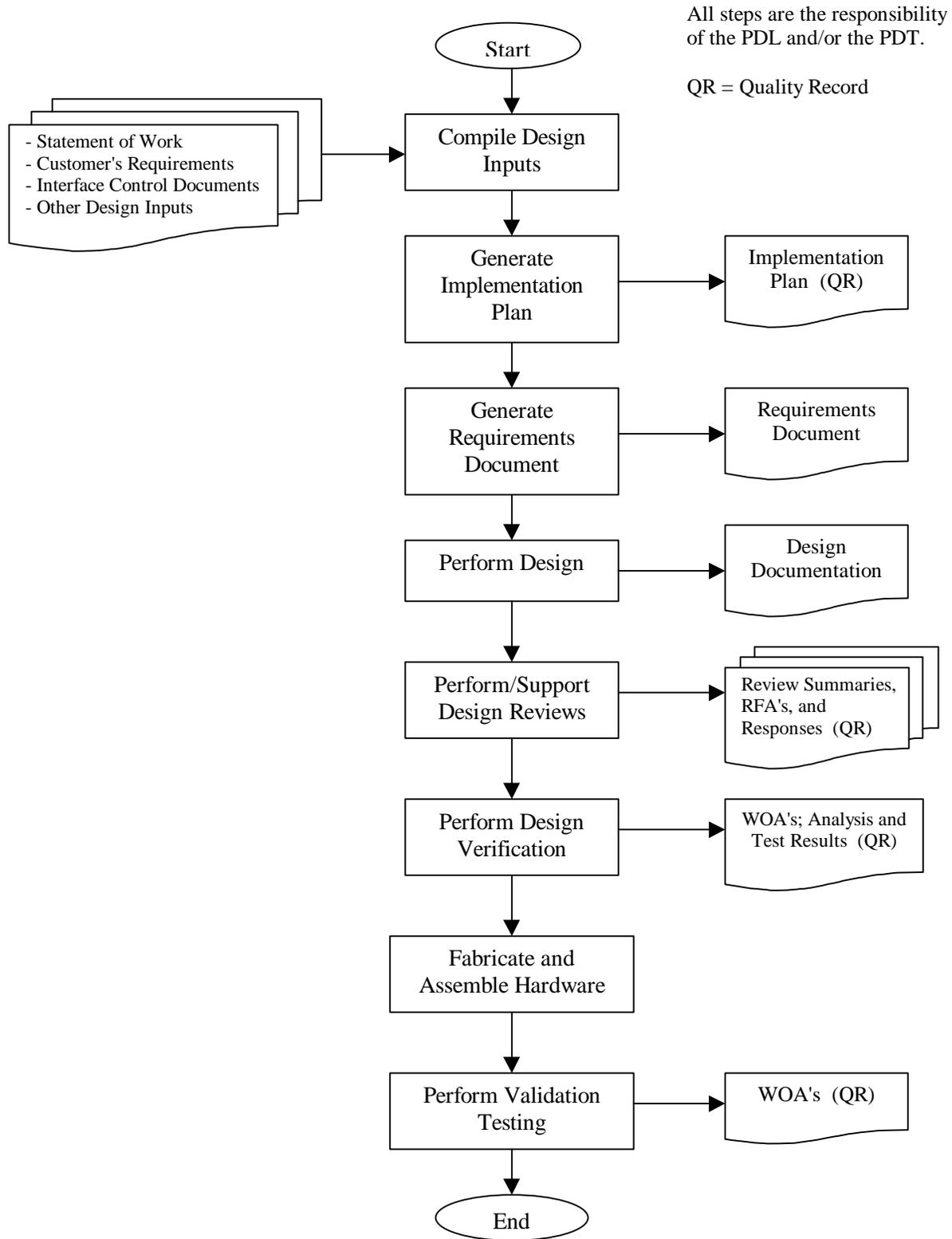
environmental tests, required for product validation. Test results shall be analyzed and evaluated to ensure that all customer imposed requirements have been validated.

8.8.5 Anomalies found during the validation process shall be documented and resolved per GPG 5340.2 (Control of Non-conforming Product) and GPG 1710.1 (Corrective and Preventive Action).

8.9 Communicating Design Output to Customer and Configuration Management

The lead engineer/PDT shall provide both the design output (engineering drawings, test plans, procedures, reports, review documentation, etc.) and the design progress (budget, schedule) to the appropriate configuration management system per GPG 8700.2, Design Development, and to the customer upon request.

9. FLOW DIAGRAM



CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
Baseline	01/14/1999	Initial Release
A	07/02/1999	Modified format to conform with GPG 1410.1A. Corrected incorrect document numbers in references. Listed references in numerical order. Clarified quality records requirements in text and flow chart. Clarified WOA usage requirements for verification and validation. Clarified drawing standards requirements for engineering test units versus flight units.